AB (Cont.)

receiving system specification information;

reusing standardized circuit block information;

performing test bench integration;

determining if a proposed circuit design passes a test;

synthesizing circuit blocks, after the proposed circuit design passes the test; and

creating a top level netlist.

Remarks

Applicant appreciates Examiner's acknowledgement of allowable material in claims 1 – 4, 5, 6, 9 – 10, 12, 14, 15.

Claims 1, 4 –8, 10, 12, 14, and 20, are objected to because of informalities. Applicants have amended claims per Examiner's suggestions and believe these objections have been addressed.

Claims 5, 11, 13, and 15 are rejected under 35 U.S.C. §112, second paragraph. Applicants have made amendments per Examiner's suggestions and believe these rejections have been addressed.

Claims 16 – 19, and 21 are rejected under 35 U.S.C. §102(b) as being anticipated by Blaner, B., et al., "RTL Design Source Management for System-on-Chip Designs. (*Blaner et al.*)" *The reference is concerned with ". . . a methodical approach to RTL design source management. Consistent adherence to a methodology consisting of project planning and management, design database management, and system verification as described . . .enables design service providers to deliver error-free silicon the meets customer specification. (Summary)*

The Applicant respectfully asserts that the Office Action's cited reference does not anticipate Applicant's claimed invention. Per MPEP §2131:

> **"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently describe in a single prior art reference."** *Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628,631,2 USPQ2d 1051, 1053 (Fed. Cir. 1987).* **The identical invention must be shown in as complete detail as contained in the . . .claim."** *Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPq2d 1913, 1920 (Fed. Cir. 1989).* **The elements must be arranged as required by the claim.**

With respect to amended claim 16, the element of *synthesizing circuit blocks* is performed as a result of a test, as defined by the next element, *determining if a proposed circuit design passes a test*. After *synthesizing circuit blocks* the claimed invention is *creating a top level netlist*. Applicant respectfully traverses the Office Action's assertion that "pg. 149, first paragraph, "Soft cores from IBM ASICs core library are delivered as technology-dependent VDHL [*sic*] or Verilog netlists," and Logic developed for the customer and chip top-level logic are coded and delivered in VDHL or Verilog form . . ." as reading as a creation of top level netlist.

The claimed invention (as shown in FIG. 17) is *synthesizing circuit blocks and creating a netlist* (1770) as a result of *determining if a proposed circuit design passes a test*(1760). The objective of the claimed invention is negated by following the procedure outlined *supra* in *Blaner et al.*

Since a *prima facie* case of anticipation has not been made, claim 16, as amended is allowable over the cited references. Since claims 17 – 19 and 21 depend upon claim 16, they are also allowable.

Claim 22 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Blaner et al.* Since claim 22 is dependent upon an allowable base claim, Applicants respectfully submit that the Office Action's rejected is rendered moot.

Claim 20 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Blaner et al* in view of *Lawman et al.* (US Patent 6,118,938). Since claim 20 is dependent upon an allowable base claim, Applicants respectfully submit that the Office Action's rejected is rendered moot.

Claims 7 – 8, and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Blaner et al* in view of *Lawman et al.* (US Patent 6,118,938) and, *Gupte et al.* (US Patent 5,903,475). Claim 7 has been cancelled. Claims 8 and 13 have been rewritten to depend upon claim 9 which has been amended per Examiner's suggestions. Applicants respectfully submit that the Office Action's rejection has been addressed.

In that claims 1 –6, and 8 – 22 are allowable as amended, Applicants respectfully request that a patent issue.

Please charge any fees other than the issue fee and credit any overpayments to Deposit Account 14-1270.

Respectfully submitted,

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APPENDIX A

Claims showing changes made. Deletions are in [brackets] and insertions are in **underline.**

1. *(Amended)* [An system on a chip] **A System on a Chip (SoC)** netlist builder and verification computer system comprising:

a user interface module for providing user friendly and convenient interfaces that facilitate easy entry and modification of user selections and parameters;

an expert system module for analyzing information supplied by said user module and automatically providing SoC building and verification data to [said] **a** parameter application module;

a parameter application module for applying parameters and developing command line strings based upon information received from said user interface and said expert system;

a chip level netlist generation module for automatically generating a chip level netlist based upon information received from said user interface module and said expert system module; and

a verification module for generating a test bench and a logical verification environment automatically including simulation models based upon information interpreted by said parameter application module.

2. *(Amended)* [The system on a chip] **The System on a Chip (SoC)** netlist builder and verification computer system of Claim 1 wherein said parameter application module creates directions passed to other modules for execution.

3 *(Amended)* [The system on a chip] **The System on a Chip (SoC)** netlist builder and verification computer system of Claim 2 wherein said directions passed to other modules for execution includes command lines.

4 *(Amended)* [The system on a chip] **The System on a Chip (SoC)** netlist builder and verification computer system of Claim 1 wherein said SoC building and verification data provided by said expert system is retrieved from a storage medium comprising a database

of building block circuit description files.

5. *(Amended)* [The system on a chip] **The System on a Chip (SoC)** netlist builder and verification computer system of Claim 1 wherein said chip level netlist generation module includes the instantiation of internal **integrated circuit (IC)** [IC] devices and connections between [the circuit blocks] **the IC devices** for internal signals.

6. *(Amended)* [The system on a chip] **The System on a Chip (SoC)** netlist builder and verification computer system of Claim 1 wherein said user interface module generates user friendly graphical user interfaces (GUIs) to facilitate selection of standardized circuit blocks and parameterization of the selected **standardized** circuit blocks.

7. *(Cancelled)* [In a computer system, an system on a chip netlist builder and verification computer method for facilitating creation and modification of IC designs utilizing existing circuit block designs, said method comprising the steps of:

providing a user friendly interface;

performing a parameter application process;

executing an expert system process;

implementing a chip level netlist generation process including core netlist and 1/0 pin netlists; and

verifying a system on a chip design automatically.]

8. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] **9** further comprising the steps of:

assisting easy entry and modification of user selections and parameters;

presenting information regarding operations of said SoC netlist builder and verification method to a user; and

facilitating selection of standardized circuit blocks and parameterization of said selected **standardized** circuit blocks.

9. *(Amended)* [The system on a chip netlist builder and verification computer method of Claim 7 further comprising the steps of:] **In a computer system, a system on a chip**

netlist builder and verification computer method for facilitating creation and modification of internal integrated circuit (IC) [IC] designs utilizing existing circuit block designs, said method comprising the steps of:

providing a user friendly interface;

performing a parameter application process;

executing an expert system process;

implementing a chip level netlist generation process including core netlist and 1/0 pin netlists;

verifying a system on a chip design automatically;

creating an underlying structure list;

interpreting information and commands entered by a user; and

performing iterations required to generate an underlying structure list.

10. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] **9** further comprising the steps of:

determining which circuit block is selected by a user;

initializing a [corresponding] **parameterizable command line** string;

processing operations for a circuit block a user has requested;

making an instance specific copy of the parameterizable command line string; and

updating a copy of the parameterizable command line string with user indicated parameters received for a particular instance.

11. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] **9** further comprising the steps of:

appending [the] circuit block attributes to other files; and

adding the gate count of a circuit block to a list of gate counts for an IC.

12. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] **9** further comprising the steps of:

generating an internal integration list associated with the circuit block **designs**; and

utilizing said internal integration list in the processing of other routines included in an SoC netlist building and verification method.

13. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] 9 further comprising the step of extracting circuit block descriptions from a storage location based upon [the] applied parameter information.

14. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] 9 further comprising the steps of:

creating an **internal integrated circuit (IC)** [IC] core level netlist in a desired location based on data

structures that were populated in other routines of said SoC netlist builder and verification computer method; and

generating hardware description language VHDL or Verilog code that automatically performs the task of coupling circuit blocks together .

15. *(Amended)* The system on a chip netlist builder and verification computer method of Claim [7] 9 further comprising the steps of:

providing signal declarations;

producing required HDL assign statements in accordance with an assignment list; and

generating the HDL code that will instantiate [each of those components] **the signal declarations and HDL assign statements** based upon an instantiation list.

16. *(Amended)* [An] A system on a chip netlist builder and verification computer method comprising the steps of:

A receiving system specification information;

B reusing standardized circuit block information;

C performing test bench integration;

D determining if a proposed circuit design passes a test;

E synthesizing circuit blocks, **after proposed circuit design passes the test**; and

F creating a top level netlist.

17. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of receiving information associated with custom designed circuit blocks.

18. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of writing a test.

19. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of facilitating communications from a user regarding circuit block selection and parameterization.

20. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 16 in which system specification information is received via a present invention **Graphical User Interface (GUI)**. [GUI.]

21. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of retrieving appropriate information from storage sources.

22. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the steps of:

generating hardware description language (HDL) files describing connections between building block circuit descriptions; and

creating external input and output hardware description language (HDL) files.

APPENDIX B

Claims remaining in application.

1. *(Amended)* A System on a Chip (SoC) netlist builder and verification computer system comprising:

a user interface module for providing user friendly and convenient interfaces that facilitate easy entry and modification of user selections and parameters;

an expert system module for analyzing information supplied by said user module and automatically providing SoC building and verification data to a parameter application module;

a parameter application module for applying parameters and developing command line strings based upon information received from said user interface and said expert system;

a chip level netlist generation module for automatically generating a chip level netlist based upon information received from said user interface module and said expert system module; and

a verification module for generating a test bench and a logical verification environment automatically including simulation models based upon information interpreted by said parameter application module.

2. *(Amended)* The System on a Chip (SoC)_netlist builder and verification computer system of Claim 1 wherein said parameter application module creates directions passed to other modules for execution.

3 *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 2 wherein said directions passed to other modules for execution includes command lines.

4 *(Amended)* The System on a Chip (SoC)_netlist builder and verification computer system of Claim 1 wherein said SoC building and verification data provided by said expert system is retrieved from a storage medium comprising a database of building block circuit

description files.

5. *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 1 wherein said chip level netlist generation module includes the instantiation of internal integrated circuit (IC) devices and connections between the IC devices for internal signals.

6. *(Amended)* The System on a Chip (SoC) netlist builder and verification computer system of Claim 1 wherein said user interface module generates user friendly graphical user interfaces (GUIs) to facilitate selection of standardized circuit blocks and parameterization of the selected standardized circuit blocks.

7. *(Cancelled)*

8. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

assisting easy entry and modification of user selections and parameters;

presenting information regarding operations of said SoC netlist builder and verification method to a user; and

facilitating selection of standardized circuit blocks and parameterization of said selected standardized circuit blocks.

9. *(Amended)* In a computer system, a system on a chip netlist builder and verification computer method for facilitating creation and modification of internal integrated circuit (IC) designs utilizing existing circuit block designs, said method comprising the steps of:

providing a user friendly interface;

performing a parameter application process;

executing an expert system process;

implementing a chip level netlist generation process including core netlist and 1/0 pin netlists;

verifying a system on a chip design automatically;

creating an underlying structure list;

interpreting information and commands entered by a user; and

performing iterations required to generate an underlying structure list.

10. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

determining which circuit block is selected by a user;

initializing a parameterizable command line string;

processing operations for a circuit block a user has requested;

making an instance specific copy of the parameterizable command line string; and

updating a copy of the parameterizable command line string with user indicated parameters received for a particular instance.

11. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

appending [the] circuit block attributes to other files; and

adding the gate count of a circuit block to a list of gate counts for an IC.

12. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

generating an internal integration list associated with the circuit block **designs**; and

utilizing said internal integration list in the processing of other routines included in an SoC netlist building and verification method.

13. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the step of extracting circuit block descriptions from a storage location based upon [the] applied parameter information.

14. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

creating an internal integrated circuit (IC) core level netlist in a desired location based on data

structures that were populated in other routines of said SoC netlist builder and

verification computer method; and

generating hardware description language VHDL or Verilog code that automatically performs the task of coupling circuit blocks together .

15. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 9 further comprising the steps of:

providing signal declarations;

producing required HDL assign statements in accordance with an assignment list; and

generating the HDL code that will instantiate the signal declarations and HDL assign statements based upon an instantiation list.

16. *(Amended)* [An] A system on a chip netlist builder and verification computer method comprising the steps of:

receiving system specification information;

reusing standardized circuit block information;

performing test bench integration;

determining if a proposed circuit design passes a test;

synthesizing circuit blocks, after the proposed circuit design passes the test; and

creating a top level netlist.

17. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of receiving information associated with custom designed circuit blocks.

18. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of writing a test.

19. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of facilitating communications from a user regarding circuit block selection and parameterization.

20. *(Amended)* The system on a chip netlist builder and verification computer method of Claim 16 in which system specification information is received via a present invention Graphical User Interface (GUI).

21. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the step of retrieving appropriate information from storage sources.

22. The system on a chip netlist builder and verification computer method of Claim 16 further comprising the steps of:

generating hardware description language (HDL) files describing connections between building block circuit descriptions; and

creating external input and output hardware description language (HDL) files.